An Efficient Sub-Frame Based Tag Identification Algorithm for UHF RFID Systems

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***Abstract*—In this paper, we propose an efficient identification algorithm for RFID systems based on EPC C1 Gen2 RFID standard[1]. Specifically, the proposed anti-collision algorithm is based on the observation of sub-frame during an identification process, and makes effective use of idle and collision statistics to accurately estimate the tag backlog and determine the proper frame size for the next inventory round. Simulation results are supplemented to demonstrate the advantages of the proposed algorithm in achieving time and computation efficiency.**

I. Introduction

Radio frequency identification (RFID) is a wireless communication technology for automatic object identification and has been widely used in logistics management, supply chain, indoor localization, manufacturing industry, etc. In most of industry solutions, passive ultra high frequency (UHF) RFID [1] is more preferable in terms of cost effectiveness, because of its long communication range, fast identification speed, large memory capacity, and low cost. A typical challenge of applying such a RFID system is to efficiently identify a large number of tags which are normally attached to a high density of products. The coexistence of various tags sharing a communication channel leads to a unique problem known as the tag collision problem [2]. Therefore, an efficient anti-collision algorithm with fast identification speed and low computation is required to identify multiple tags when its number is extremely large.

Technically, there are two categories of anti-collision algorithms for solving RFID multiple-access problem: tree-based [3][4] and Aloha-based [5][6]. The essence of the tree-based algorithm is a collision bit identification and tracking techniques. However, it is extremely difficult to be implemented in EPC C1 Gen2 [7] or ISO 18000-6B [8] based UHF RFID systems, because of the wide deviation of received signals at a reader which cannot efficiently detect bits collision positions in a large scale. For example, in EPC C1 Gen2 standard, the symbol rate deviations of modulation signals may up to $\pm 22\%$ between tags [7][9], which causes arrival times of different tag responses vary greatly in a range of 24 microseconds (µs). Similarly, in ISO 18000-6B standard, the symbol rates of tags also deviate up to $\pm 15\%$. As a contrary, the Aloha-based anti-collision algorithm is more suitable for UHF RFID systems, since it does not necessarily to identify collision positions. Hence, it is widely implemented in practical UHF RFID system.

Specifically, dynamic frame slotted Aloha (DFSA), a popular version of Aloha-based algorithm, is specified by the EPC C1 Gen2, and widely applied in UHF RFID systems. The performance of DFSA depends on both the estimation of tag backlog (unread tags) and the setting of frame size. However, to increase the estimation accuracy, most of the existing anti-collision algorithms [5][6] require too much computation load or large amount of memory.

There are some state-of-art works on the implementation of DFSA algorithm [10][11], which can be applied into a computation-limited reader. Chen in [10] proposes a simple but relatively accurate method (FEIA) for tag backlog estimation. However, the procedures of the estimation and frame size adjustment should be performed at every time slot, which causes a heavy loading for a mobile reader with limited computation capability. Moreover, the FEIA is constrained by the scenario that the initial slot should not be idle during a frame. To achieve the energy saving of the reader, Solic et al. in [11] propose an Improved Linearized Combinatorial Model (ILCM) that only brings a modest floating point operations (FLOP) cost, and can be easily implemented as a tag backlog estimation method. It significantly reduces the computation energy consumption of the estimation, nonetheless, its performance is deteriorated with the increasing number of tags.

To reduce the computation complexity and guarantee the reliable identification performance of DFSA, we propose an efficient tag identification algorithm named sub-frame based dynamic frame slotted aloha (SUBF-DFSA) for the EPC C1 Gen2 standard. The proposed algorithm predicts the next frame size based on the observation of the current sub-frame, in which the probability relations between idle and collision for an expected system throughput is provided to improve the effectiveness of the backlog estimation. Moreover, consider the disparity between slot durations, the traditional system throughput metric (the ratio between the number of tags and the total slots required) [5][10] may be ineffective in terms of

[1]EPCglobal UHF Class-1 Generation-2 (EPC C1 Gen2) is a most used specification for RFID air interface, which defines the physical and logical requirements for a RFID system operating in the 860MHz-960MHz frequency range. The specification also defines the basic anti-collision algorithm named Q-algorithm.

identification time to evaluate the performance of anti-collision algorithms. Therefore, the average identification time has been taken into account in our scheme. In essence, compared to existing algorithms, the proposed scheme can achieve much better time efficiency, faster identification speed, and lower computation complexity.

II. Algorithm Description

The proposed anti-collision algorithm consists of two parts:optimal frame size adjustment and tag backlog estimation. Specifically, the reader makes effective use of idle and collision statistics to estimate the backlog by using only a fraction of the current frame. And then, the reader adjusts an optimal frame size for an estimated backlog. The above identification round repeats until all tags are successfully identified.

A. The adjustment strategy of frame size

Most existing algorithms solve the collision and adjust the next frame size by estimating a tag backlog according to the last full frame size. However, standards such as EPC C1 Gen2 specifies an in-frame adjustment of frame size by using the QueryAdj command. The main advantage of Q-algorithm is its simplicity of implementation in RFID system. However, the adjustment strategy is not explained in details in the standard and fails to cope with application scenarios when the number of tags varies in a wide range.

Therefore, we propose an efficient algorithm to decide the next frame size using a proportion (called a sub-frame F_{sub}) of the full frame. After reading of the sub-frame, the reader computes the ratio between the probability of being idle to that of a collision during the sub-frame. If the ratio exceeds an applicable threshold range, the reader will adjust the next frame size based on the measurement over the sub-frame. The threshold defines the upper and lower bounds of the ratio. We assume that n tags need to be identified with a frame size F: with a total of F slots, the system throughput is given by [5]:

$$U = \left(\frac{n}{F}\right) \cdot \left(1 - \frac{1}{F}\right)^{n-1} \tag{1}$$

The maximum throughput can be obtained when the frame size equals to the number of tags ($F = n$). As specified by the EPC C1 Gen2 standard, the frame size is limited to 2^Q (Q is an integer from 0 to 15). In order to avoid performance degradation, we derive the appropriate frame sizes for different estimated tag backlogs. Given a value of n, we define that the throughput of frame size F_L ($F_L = 2^Q$) equals to that of the throughput of F_H ($F_H = 2^{Q+1}$), and have

$$\left(\frac{n}{F_L}\right) \cdot \left(1 - \frac{1}{F_L}\right)^{n-1} = \left(\frac{n}{F_H}\right) \cdot \left(1 - \frac{1}{F_H}\right)^{n-1} \tag{2}$$

Therefore, the critical value n to determine whether the reader should adjusts the frame length can be derived as

$$n = \left\lfloor 1 + \frac{\ln\left(\frac{F_H}{F_L}\right)}{\ln\left(\frac{F_L}{F_H} \cdot \frac{F_H - 1}{F_L - 1}\right)} \right\rfloor \tag{3}$$

where $\lfloor * \rfloor$ represents round down to the nearest integer. Tab. I summarizes the optimal F_{nxt} (next full frame size) for different estimated tag backlog range. It is noted that the authors in [12] provide another Q-selection method which can yield the same result. But our scheme is simpler without multiple loop iterations.

TABLE I
Relation Between Optimal Frame Size and Tag Backlog Range

Estimated tag backlog range (n_1 to n_2)	Optimal frame size (F=2^Q)	Q ($\log_2^F$)
1 to 3	2	1
4 to 5	4	2
6 to 11	8	3
12 to 22	16	4
23 to 44	32	5
45 to 89	64	6
90 to 177	128	7
178 to 355	256	8
356 to 710	512	9
711 to 1420	1024	10
1421 to 2839	2048	11
2840 to 5678	4096	12
5679 to 11357	8192	13
11358 to 22713	16384	14
22714 to 45426	32768	15

B. The backlog estimation method

P_e and P_c denote the probabilities of idle and collision, respectively. It is concluded that the throughput (U) is a convex function, whereas P_e and P_c are decreasing and increasing functions, respectively. Now, we describe our estimation method.

It is proved that the optimal DFSA can achieve the highest throughput of 0.368, given that the frame size is properly adjusted [5]. We thus make a reasonable assumption to ensure a high average system throughput U, i.e., $U \geq 0.35$, and calculate the probability ranges of Pe and Pc for different values of F_{cur} and n_{est}, where F_{cur} denotes the current full frame size, nest denotes the current estimated tag quantity, using the following procedure. The result is provided in Tab. II.

Initialize Q=4, $i = 1$, $C_f = \log_2^{(n_{est}/F_{cur})}$;

Note that each C_f corresponds a case of the following Tab. II.
1) while ($Q \leq 15$) // according to Tab. I, to calculate all estimated probability relation
{ $F = 2^Q$, $Q_f = Q + Q_f$, n_1, n_2 (refer to the value of $Q = Q_f$ in Tab. I)
$P_e\left(n_2\right)/P_c\left(n_2\right) = a_i$, where $P_e = (1 - 1/F)^n$, $P_c = 1 - P_e - U$
$A_i <= a_i \cdot P_c \leq P_e \leq b_i \cdot P_c$, $Q++$, $i++$
2) Averaging all A_i, leads to the average estimation
$a_i \cdot P_c \leq P_e \leq b_i \cdot P_c$ in Tab. II

Considering the first m-slots ($F_{sub} = m$) of a full frame, the ratio between the probability of idle and that of collision during a sub-frame is $m \cdot P_e / m \cdot P_c = P_e / P_c$, which equals to the ratio between the probability of idle and that of collision during the full frame. Therefore, the results in Tab. II are

TABLE II
THE RELATION BETWEEN P_e AND P_c FOR DIFFERENT VALUES OF F_{cur} AND n_{est}

n_{est} vs. F_{cur}	Relation between P_e and P_c
$n_{est} = F_{cur}/4 \ (C_f = -2)$	$15.1P_c < P_e \leq 63.8P_c$
$n_{est} = F_{cur}/2 \ (C_f = -1)$	$3.2P_c < P_e \leq 15.1P_c$
$n_{est} = F_{cur} \ (C_f = 0)$	$0.6P_c < P_e \leq 3.2P_c$
$n_{est} = 2F_{cur} \ (C_f = 1)$	$0.08P_c < P_e \leq 0.6P_c$
$n_{est} = 4F_{cur} \ (C_f = 2)$	$0 \leq P_e \leq 0.08P_c$

suitable for variety sizes of sub-frame even full frame included. Simulation results are supplemented to verify the effectiveness of the proposed solution.

With the probability relations of P_e and P_c in Tab. II, we can adjust F to be suitable for n by keeping track of the ratio between P_e and P_c during the sub-frame which is provided by the reader. For example, if the reader computes that $3.2P_c < P_e \leq 15.1P_c$ during the identification process of a sub-frame, it presumes that n_{est}=$F_{cur}/2$ and estimates the tag backlog as $(F_{cur}/2) - S_{sub}$, where S_{sub} is the successful slots (identified tags) during the sub-frame. It is noted that if there is no collision in a sub-frame, i.e. P_c=0, we should set tag backlog as $(F_{cur}/2) - S_{sub}$.

C. The proposed tag identification algorithm

Combining the adjustment strategy of frame size and estimation method, we propose the anti-collision algorithm SUBF-DFSA as follows:

Algorithm SUBF-DFSA

1. Initialize $F_{cur} = F_{ini}$, F_{sub}, P_e, and P_c;
2. where F_{ini} and F_{sub} are initial full frame and sub-frame size, respectively
3. **while** (unidentified tags $\neq 0$)
4. Each tag selects a time slot randomly among F_{cur} slots and transmits its data to the reader slot by slot
5. Compute P_e/P_c after the reading of F_{sub} slots, where P_e and P_c are probabilities of idle and collision during F_{sub} slots, respectively
6. Select one case from Tab. II and judge whether the case satisfied
7. **if** the case is satisfied
8. Perform the estimation according to Tab. II and adjust a new frame size $F_{cur} = F_{nxt}$ according to Tab. I, and update F_{sub}
9. **else**
10. Repeat step 6 until all cases are examined
11. end **if**
12. end **while**

where F_{sub} should be set as $F/2^k$ (k is an integer), i.e., $F/2$, $F/4$, $F/8$, $F/16$ etc., since the size of full-frame F is 2^Q. If $F_{cur} < 2^k$, F_{sub} should be set as min(4, F_{cur}), since F_{sub} should be power of 2 and contain at least idle, collision and successful slot to estimate backlog according to Tab. I. Noting that F is not fixed but varies for every identification round. We will compare the time efficiency for different sub-frame sizes and find out which one can lead to better performance.

III. SIMULATION RESULTS

We evaluate the time efficiency and average identification time of the proposed algorithm, and compare its performance with existing methods including Maximum a posteriori estimation (MAP) [5], FEIA [10], and ILCM [11] over extensive Monte Carlo simulations. According to the EPC C1 Gen2 specification, the time efficiency $T_{efficency}$ is defined as

$$T_{efficiency} = \frac{S \cdot T_{succ}}{T_{slots} + T_{FLOP}} \tag{4}$$

$$T_{slots} = S \cdot T_{succ} + E \cdot T_{idle} + C \cdot T_{coll} \tag{5}$$

where S, E, and C are the number of occurrence in success, idle, and collision of an inventory process, respectively. T_{succ}, T_{idle} and T_{coll} are the time durations for each case above and have

$$T_{idle} = T_{cmd} + T_1 + T_3 \tag{6}$$

$$\begin{aligned} T_{succ} = T_{cmd} + 2\left(T_1 + T_2\right) + T_{RN16} \\ +T_{ACK} + T_{PC+EPC+CRC} \end{aligned} \tag{7}$$

$$T_{coll} = T_{cmd} + T_1 + T_{RN16} + T_2 \tag{8}$$

where T_{cmd} is the time duration of reader's inventory command which can be Query, QueryAdj, or QueryRep [7].

$$T_{FLOP} = \frac{\left(\sum_{i=1}^{T_{sw}} N_{FLOP}^{i}\right)}{R_{FLOPS}} \tag{9}$$

where T_{sw} denotes the number of rounds, which is counted by the reader during the whole identification process. Consider a portable RFID reader with an embedded processor, such as ARM AT91SAM7S256, its floating point operation ability is highly constrained, compared to multi-core processors which are used in smart phone or personal computer. We consider the FLOP cost which is another key requirement that needs to be taken into account in the design of anti-collision algorithm. The higher the computation complexity, the larger the value of N_{FLOP}^{i}, which denotes the floating point operation cost of a reader in i-th inventory round. R_{FLOPS} represents the reader's computational power of k MFLOPS (10^6 floating point operations per second). In our simulation, we set k[2] as 6.

To obtain the average time for identifying one tag $(\left(\frac{T_{slots}+T_{FLOP}}{n}\right))$, we need to calculate the time duration of every step in (6), (7), (8), and FLOP (9) used in the anti-collision process. For a fair comparison, the primary time parameters, i.e., T_1, T_2, T_3, T_{Query}, $T_{QueryRep}$, $T_{QueryAdj}$, T_{RN16}, T_{ACK}, $T_{PC+EPC+CRC}$, etc., used in the simulations are the same as in [10]. It is noted that to evaluate the total FLOP cost, we use the reference values presented in [11][12], given in Tab. III (a), and Tab. III (b) summarizes the approximate number of FLOP required to identify 1000 tags under various algorithms with an initial frame size 32.

The FLOP cost of anti-collision algorithm derives from the tag backlog estimation and frame size setting in the process of identification. MAP involves optimization of arithmetical

[2] The computation capability of ARM processor with a single-core architecture is between 0.3∼6 MFLOPS. The proposed algorithm can better cope computation limitations, however, as a fair comparisons with existing solutions, we choose a maximum value of 6.

TABLE III
COMPARISON OF COMPUTATION COMPLEXITY

(a) FLOP cost for each operation

Operation	FLOP cost
Addition, subtraction, multiplication	1
Comparison operation	2
Division, square root	10
Exponential, logarithmic and trigonometric function	50
Factorial	100

(b) Total FLOP cost of various algorithm

Algorithm	Total FLOP cost
MAP	2.03×10^6
FEIA	4.39×10^4
ILCM	1.44×10^4
SUBF-DFSA	2.07×10^3
Q-algorithm	1.80×10^3

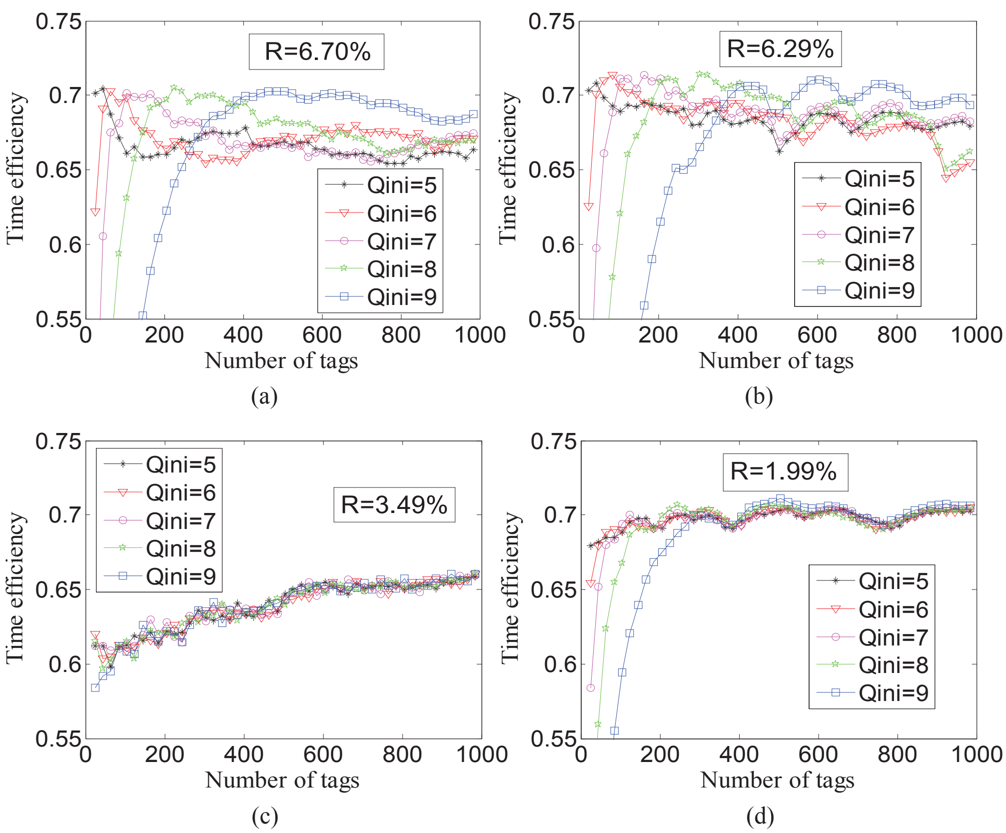

Fig. 1. Influence of initial frame size on the time efficiency. (a) MAP estimation (b) ILCM (c) FEIA (d) SUBF-DFSA

operation which requires the vast number of searches. Hence, the complexity of MAP is highest. FEIA provides a relatively simple estimation method. Compared to MAP, the FLOP cost of FEIA is reduced. However, the procedures of the estimation and frame size adjustment should be performed at every time slot, which also causes a heavy loading for a reader with low hardware cost. ILCM only performs one estimation at each identification round. However, the estimation includes exponential, trigonometric function with higher FLOP cost. Compared to the above algorithms, the frame size setting and estimation of SUBF-DFSA are achieved by Tabs. I and II. Only one estimation implemented at each identification round. Furthermore, SUBF-DFSA only involves addition, multiplication and comparison operations, the complexity of SUBF-DFSA is significantly reduced.

We first compare the reliability of various anti-collision algorithms with different initial frame size in Fig. 1. The fluctuate ratio of variables (e.g. time efficiency or average identification time) can be defined as

$$R = \frac{|V_{avg} - V_{\max}|}{V_{avg}} \tag{10}$$

where V_{avg} and V_{max} denote the average and maximum value of variables when the number of tags varies from 25 to 1000 in step of 20 with an initial frame size of 32, 64, 128, 256, and 512, respectively. As can be seen from Fig. 1 (a) and (b), the performance of MAP and ILCM are significantly affected by the initial frame size. When the number of tags is large and the frame size is small, both methods are unable to adjust the appropriate frame size to fit the tag backlog, and cause performance deterioration. In other words, the

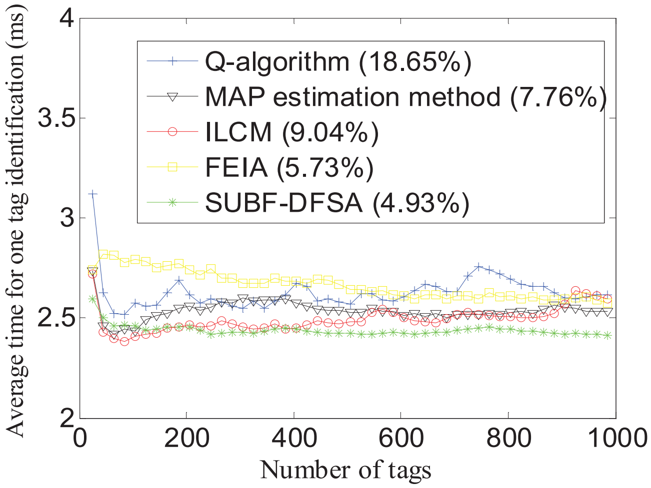

Fig. 2. Average time required for identifying one tag

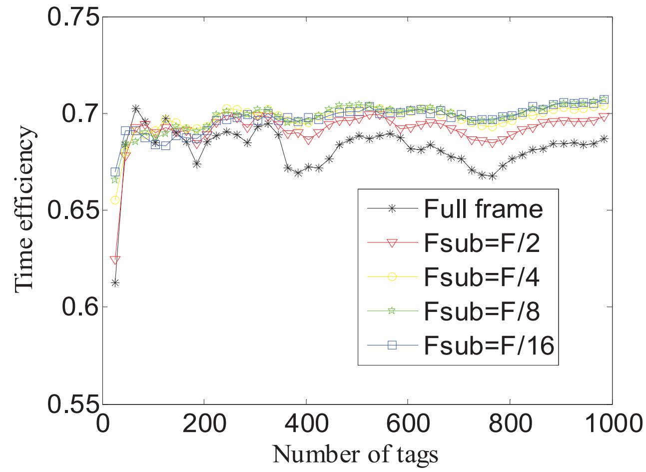

Fig. 3. Comparison of time efficiency for different sub-frame size

stability and scalability of these methods are poor to adapt to a wide range of tags. Compared to MAP and ILCM, the time efficiency of FEIA in Fig. 1(c) is almost independent to the initial frame size, which means FEIA can efficiently adapt the frame size to the current tag backlog. However, the performance remains on a low efficiency when the number of tags is relatively small. This is because the algorithm estimates the tag backlog at every time slot by using the observation from previous slots. When the number of previous slots is small, the estimation becomes inaccurate and thus affects the identification performance. Fig. 1(d) shows the performance of the proposed SUBF-DFSA with $F_{sub} = F/8$, as can be seen when the number of tags is greater than 200, time efficiencies of varied frame sizes can constantly converge to 0.7034. With our algorithm, the reader is allowed to accurately adjust the inappropriate frame size according to the observation from sub-frame to achieve a stable identification efficiency.

Fig. 2 presents the simulation result of the average time required to identify one tag with an initial frame size of 64. The average time includes communication time between tags and the reader, and processing time of the reader which is limited by the hardware capability. As can be seen, the proposed algorithm spends about 2.45ms, i.e., an identification speed is of 408 tags/s. The identification speed of our scheme is hardly affected by the number of tags. Compared to reference methods, our algorithm can maintain a stable performance. For example, when the number of tags is less than 300, ILCM performs good due to the low computations and efficient estimation. However, as the number of tags increases, its performance deteriorates. By contrast, FEIA can achieve a high identification speed when the number of tags is large because average FLOP cost required is more balanced as the number of tags increases. When the number of tags is relatively small, the adjustment times is overwhelmed and negatively affect the identification speed. Fig. 3 presents the time efficiency for different F_{sub}. The initial frame size is also set to 64. It is observed that the proposed sub-frame method is better than the traditional full frame method. Moreover, there is a slight difference between the cases of the sub-frame size of $F/4$, $F/8$, and $F/16$. The optimal choice of sub-frame size depends on system settings, such as frame size and number of tags. In our experiments, $F/8$ strikes the good average performance and reliability when the number of tags varies in a large scale, which is suitable for all values of Q_{ini}.

TABLE IV
COMPARISON OF SYSTEM THROUGHPUT FOR VARIOUS ALGORITHMS

Method	Average ($25 \leq n \leq 1000$)	Improvement
Q-algorithm	0.2950	-
ILCM	0.3272	10.92%
FEIA	0.3322	12.61%
MAP estimation	0.3356	13.76%
SUBF-DFSA	0.3489	18.27%

In order to make fair comparisons with existing literatures, Tab. IV summarizes the average performance of various algorithms in term of system throughput and its improvement percentages over that of Q-algorithm when an initial frame size set to 32, 64, 128, 256, and 512, respectively.It is noted that although the system throughput of ILCM is lower than that of FEIA and MAP estimation methods, the computation complexity of ILCM is much lower than them. Hence, the performance of ILCM are better than above two algorithms in terms of time efficiency and average time to identify one tag which take computation complexity into account.

Basically, read speed, fluctuation ratio, and computation complexity are three key criteria for evaluating a RFID system. To fully show the performance advantage of the proposed algorithm, the Tab. V compares the overall performance of various anti-collision algorithms. Noting that the numbers inside the brackets in each column representing the individual performance ranking. As can be observed from Tab. V, although the proposed SUBF-DFSA is not best in all three performance metrics, it still can achieve the best overall performance. Also, since our proposed algorithm is based on

TABLE V
RELATION BETWEEN OPTIMAL FRAME SIZE AND TAG BACKLOG RANGE

Method	Read speed	Fluctuate ratio of time efficiency	Computation complexity	Overall ranking
Q-algorithm	361 (5)	7.29% (5)	0.9×10^3 (1)	4
MAP estimation	381 (3)	6.70% (4)	6.3×10^5 (5)	5
ILCM	386 (2)	6.29% (3)	1.44×10^4 (3)	2
FEIA	375 (4)	3.49% (2)	4.39×10^4 (4)	3
SUBF-DFSA	410 (1)	1.99% (1)	2.07×10^3 (2)	1

the same hardware platform of Q-algorithm, it will not bring in extra requirements compared to other algorithms.

IV. CONCLUSION

We proposed an efficient anti-collision algorithm with good performance for the EPC C1 Gen2 standard. The proposed scheme is based on the observation of sub-frame during an identification procedure with frame size F. Performance comparisons show the advantages of our proposed algorithm in achieving fast identification speed, high stability, and low computational complexity, which is helpful to design new mobile RFID readers with low hardware overhead.

Based on the promising results, future research activities will go in the challenging direction of extending the algorithm to consider the effect of channel errors, to implement the algorithm into the practical RFID hardware platform, and demonstrate the implementation results.

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